Claims:

1. A packaged IC comprising:
an IC die,
a signal trace and a signal complement trace positioned relative to each other to maximize broadside coupling for a matching impedance, said signal and signal complement traces separated by a dielectric coupling layer, and electrically connected to pads on said IC die,
a signal trace conductive reference layer separated from said signal trace by signal trace dielectric isolation layer, and
a signal complement trace conductive reference layer separated from said signal complement trace by signal complement trace dielectric isolation layer.

2. A packaged IC as recited in claim 1 wherein said dielectric coupling layer and said signal and signal complement trace dielectric isolation layers are ceramic.

3. A packaged IC as recited in claim 1 wherein said matching impedance has a value of approximately 50 ohms.

4. A packaged IC as recited in claim 3 wherein said dielectric coupling layer and said signal and signal complement trace dielectric isolation layers are ceramic, said signal and said signal complement traces have a width of approximately 80 microns, said signal and signal complement traces are separated from each other a distance of

approximately 300 micrometers, and said signal and signal complement dielectric isolation layers are separated from said signal and signal complement traces by approximately 300 microns.

5. A packaged IC as recited in claim 1 wherein said signal trace and said signal complement trace are substantially parallel with each other.

6. A packaged IC as recited in claim 1 and further comprising via pairs wherein said via pairs are connected to said signal trace and said signal complement trace and are adjacent each other.

7. A packaged IC as recited in claim 6 wherein said via pairs are adjacent to a first via electrically connected to said signal trace conductive reference layer and a second via electrically connected to said signal complement trace conductive reference layer.

8. A packaged IC as recited in claim 1 wherein said signal and signal complement traces electrically connect to a clock signal on said IC die.

9. A packaged IC as recited in claim 8 wherein access to said clock signal is in a center of said IC package.

10. A packaged IC as recited in claim 8 wherein a plurality of signal and signal complement traces deliver said clock signal from an access to said clock signal on said IC die to a plurality of

locations on said packaged IC, each of said plurality of signal and signal complement traces having substantially equivalent trace lengths.

11. A packaged IC as recited in claim 3 disposed on a circuit board, said circuit board having 50 ohm circuit board traces wherein leads on said IC package that are electrically connected to said signal and signal complement traces are connected to said 50 ohm circuit board traces.

12. A packaged IC as recited in claim 1 wherein said signal trace comprises a first signal trace and said signal complement trace comprises a first signal complement trace and further comprising second signal and second signal complement traces positioned to maximize edge-side coupling and separated from said signal trace conductive reference layer by a second dielectric isolation layer.

13. A packaged IC as recited in claim 1 wherein said signal trace comprises a first signal trace and said signal complement trace comprises a first signal complement trace and further comprising second signal and second signal complement traces separated by a second dielectric coupling layer, said second signal and signal complement traces positioned relative each other to maximize broadside coupling wherein said first electrically conductive reference layer is positioned intermediate said first signal and signal complement traces and said second signal and signal complement traces and is separated from

said second signal trace by a second signal trace dielectric isolation layer and further comprising a second signal complement trace conductive reference layer positioned on an opposite side of said second signal and signal complement traces separated from said second signal complement trace by a second signal complement trace dielectric isolation layer.

14. A packaged IC as recited in claim 13 and further comprising any number of additional signal and signal complement traces, each separated by a dielectric coupling layer and positioned to maximize broadside coupling, said additional signal and signal complement traces sharing a signal trace conductive reference layer with another signal and signal complement trace pair on at least one side and having corresponding signal trace and signal complement trace dielectric layers separating said signal and signal complement traces from said signal and signal complement trace conductive reference layers.

15. A method of manufacturing a packaged IC comprising the steps of:

calculating trace width and spacing requirements of one or more signal and signal complement traces for a matching impedance at a given dielectric constant using broadside coupling in an IC package design,

positioning said one or more signal and signal complement traces to maximize broadside coupling according to said step of calculating in an IC package design,

positioning one or more signal and signal complement trace conductive reference layers parallel to said signal and signal complement traces separated by signal and signal complement trace dielectric isolation layers in an IC package design,

manufacturing an IC package according to said IC package design, and

electrically connecting pads on an IC die to said signal and signal complement traces of said IC package.

16. A method of manufacturing as recited in claim 15 wherein said IC package design wherein said signal trace, signal complement trace, dielectric coupling layer, signal and signal complement trace dielectric isolation layers, and signal and signal complement trace conductive reference layers comprises a signal routing layer and said IC design comprises at least two routing layers.

17. A method of manufacturing as recited in claim 15 wherein said step of calculating is performed for a ceramic dielectric.

18. A method of manufacturing as recited in claim 15 wherein said steps are performed for said matching impedance having a value of 50 ohms.

19. A method of manufacturing as recited in claim 15 and further comprising the step of connecting said signal and said signal complement traces to via pairs, wherein said via pairs are adjacent each other.

20. A method of manufacturing as recited in claim 15 and further comprising the step of electrically connecting said signal and signal complement traces to a clock signal access on said IC package.

21. A method of manufacturing as recited in claim 20 and further comprising the step of positioning a plurality of signal and signal complement traces from said clock signal access to a respective plurality of locations on said IC package wherein all of said signal and signal complement traces have substantially the same length.

22. A method of manufacturing as recited in claim 15, wherein said packaged IC die is disposed on a circuit board having 50 ohm circuit board traces wherein leads on said IC package that are electrically connected to said one or more signal

and signal complement traces are connected to said 50 ohm circuit board traces.

23. A method of manufacturing as recited in claim 15 wherein said signal and signal complement traces comprise first signal and signal complement traces and further comprising the step of positioning second signal and signal complement traces to maximize edge-side coupling, separated from said signal trace conductive reference layer by a second signal trace dielectric isolation layer.

24. An IC die comprising:
a plurality of first signal and signal complement die pads comprising a die pad pair, each first signal and signal complement die pad pair aligned along parallel lines that are perpendicular to a die edge, said plurality of first signal and signal complement pads being adjacent said die edge,
a plurality of second signal and signal complement die pads aligned along said parallel lines that are perpendicular to said die edge, said plurality of second signal and signal complement die pads being on an opposite side of said plurality of first signal and signal complement pads from said die edge.

25. An IC die as recited in claim 24 and further comprising any number of additional pluralities of signal and signal complement die pads, each signal and signal complement die pad pair aligned along said parallel lines.

26. An IC die as recited in claim 24 wherein each said signal and signal complement die pad pair further comprises a reference and bias pad aligned along said parallel lines.

27. An IC die as recited in claim 26 wherein said signal, signal complement, reference, and bias pads comprise a single signal pad unit and wherein each signal pad unit is either a receive signal pad unit or a transmit signal pad unit and wherein said reference and bias pads of a receive signal pad unit are closest to said signal and signal complement pads of an adjacent parallel one of said transmit pad units.

28. An IC die as recited in claim 26 wherein said signal, signal complement, reference, and bias pads comprise a single signal pad unit and wherein each signal pad unit is either a receive signal pad unit or a transmit signal pad unit and wherein said transmit signal and signal complement pads are positioned as far away as possible from said receive signal and signal complement pads.

29. A method for laying out an IC comprising the steps of:

positioning a plurality of first signal and signal complement pads, each first signal and signal complement pad pair aligned along parallel lines that are perpendicular to a die edge, said plurality of first signal and signal complement pads being adjacent said die edge,

positioning a plurality of second signal and signal complement pads aligned along said parallel lines that are perpendicular to said die edge, said plurality of second signal and signal complement pads being on an opposite side of said plurality of first signal and signal complement pads from said die edge.

30. A method for laying out an IC as recited in claim 29 and further comprising the step of positioning any number of additional pluralities of signal and signal complement pads, each signal and signal complement pad pair aligned along said parallel lines.

31. A method for laying out an IC die as recited in claim 29 and further comprising the step of positioning a reference and a bias pad aligned along said parallel lines.

32. A method for laying out an IC die as recited in claim 31 wherein said signal, signal complement, reference, and bias pads comprise a single signal pad unit and wherein each signal pad unit is either a receive signal pad unit or a transmit signal pad unit and further comprising the step of positioning said reference and bias pads of a receive signal pad unit closest to said signal and signal complement pads of an adjacent parallel one of said transmit pad units.

33. An IC die as recited in claim 31 wherein said signal, signal complement, reference, and bias pads

comprise a single signal pad unit and wherein each signal pad unit is either a receive signal pad unit or a transmit signal pad unit and further comprising the step of positioning said transmit signal and signal complement pads as far away as possible from said receive signal and signal complement pads.